



BGA7210

700 MHz to 3800 MHz high linearity variable gain amplifier

Rev. 5 — 20 January 2017

Product data sheet

1. Product profile

1.1 General description

The BGA7210 MMIC is, also known as the BTS6001A, an extremely linear Variable Gain Amplifier (VGA), operating from 0.7 GHz to 3.8 GHz. The maximum gain is 30 dB. It has an attenuation range of 31.5 dB. At its minimum attenuation setting it has a maximum output power of 21 dBm, an $IP3_O$ of 39 dBm and a noise figure of 6.5 dB.

The current consumption can be optimized per attenuation setting allowing for optimized overall system performance. The current consumption and attenuation level are controlled through a Serial Peripheral Interface (SPI). The current can be reduced to 120 mA. Optimal linearity performance is obtained at 185 mA. The BGA7210 has a fast switching power-down pin to further reduce current consumption during idle time.

The BGA7210 has been designed and qualified for the severe mission profile of cellular base stations, but its outstanding RF performance and interfacing flexibility make it suitable for a wide variety of applications.

The BGA7210 is housed in a 32 pins 5 mm × 5 mm leadless HVQFN32 package.

1.2 Features and benefits

- Operating frequency range from 0.7 GHz to 3.8 GHz
- High gain of 30 dB
- High $IP3_O$ of 39 dBm
- Attenuation range of 31.5 dB with 0.5 dB step (6 bit)
- Maximum output power of 21 dBm
- Noise figure of 6.5 dB at maximum gain
- ESD protection on all pins (HBM 4 kV; CDM 2 kV)
- Fast switching power-save mode
- Moisture sensitivity level 1
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- IF and RF applications
- WiMAX and cellular base stations
- Cable modem termination systems
- Temperature compensation circuits



1.4 Quick reference data

Table 1. Quick reference data

$4.75\text{ V} \leq V_{\text{SUP}} \leq 5.25\text{ V}$; $-40\text{ }^{\circ}\text{C} \leq T_{\text{amb}} \leq +85\text{ }^{\circ}\text{C}$; maximum current; input and output is terminated with $50\text{ }\Omega$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SUP}	supply voltage		[1] 4.75	5.0	5.25	V
$I_{\text{CC(tot)}}$	total supply current	maximum current	160	195	230	mA
		optimized current	[2] -	185	-	mA
		minimum current	-	120	-	mA
		power-down current	-	15	-	mA
T_{amb}	ambient temperature		-40	+25	+85	$^{\circ}\text{C}$
G_{p}	power gain	minimum attenuation				
		$700\text{ MHz} \leq f \leq 1400\text{ MHz}$	26	30	33	dB
		$1400\text{ MHz} \leq f \leq 1700\text{ MHz}$	26	29.5	33	dB
		$1700\text{ MHz} \leq f \leq 2200\text{ MHz}$	26	29	33	dB
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	25	28	31	dB
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	22	26	30	dB
α_{range}	attenuation range	$700\text{ MHz} \leq f \leq 2200\text{ MHz}$	28	31.5	35	dB
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	27	30.5	34	dB
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	26	29.5	33	dB
NF	noise figure	minimum attenuation				
		$700\text{ MHz} \leq f \leq 2200\text{ MHz}$	-	6.5	8.5	dB
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	-	7	9	dB
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	-	8	10	dB
		maximum attenuation				
		$700\text{ MHz} \leq f \leq 2200\text{ MHz}$	-	27.5	30.5	dB
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	-	28	31	dB
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	-	28.5	32	dB
IP3 _O	output third-order intercept point	minimum attenuation	[3]			
		$700\text{ MHz} \leq f \leq 1400\text{ MHz}$	34	39	-	dBm
		$1400\text{ MHz} \leq f \leq 1700\text{ MHz}$	32	37	-	dBm
		$1700\text{ MHz} \leq f \leq 2200\text{ MHz}$	30	35	-	dBm
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	28	34	-	dBm
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$; $C_{\text{sh}} = 0.68\text{ pF}$	[4] 30	35	-	dBm
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	24	30	-	dBm
		maximum attenuation	[3]			
		$700\text{ MHz} \leq f \leq 1400\text{ MHz}$	-	35	-	dBm
		$1400\text{ MHz} \leq f \leq 1700\text{ MHz}$	-	33	-	dBm
		$1700\text{ MHz} \leq f \leq 2200\text{ MHz}$	-	31	-	dBm
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	-	30	-	dBm
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$; $C_{\text{sh}} = 0.68\text{ pF}$	[4] -	30	-	dBm
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	-	25	-	dBm

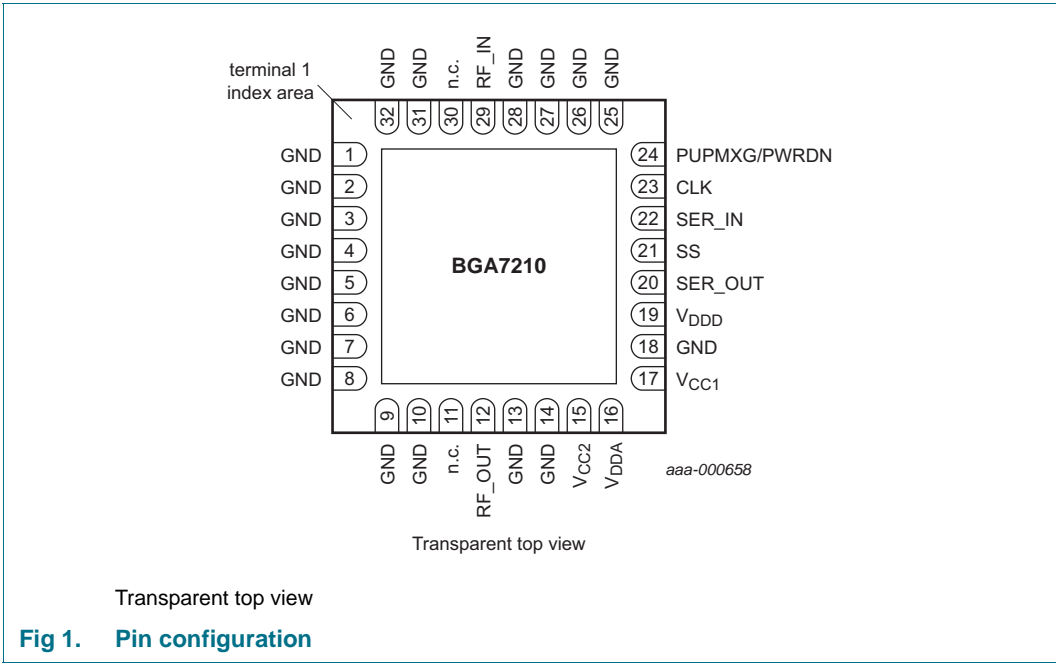
Table 1. Quick reference data ...continued
4.75 V ≤ V_{SUP} ≤ 5.25 V; −40 °C ≤ T_{amb} ≤ +85 °C; maximum current; input and output is terminated with 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P _{L(1dB)}	output power at 1 dB gain compression	minimum attenuation				
		700 MHz ≤ f ≤ 2800 MHz	18	21	-	dBm
		2200 MHz ≤ f ≤ 2800 MHz; C _{sh} = 0.68 pF [4]	20	23	-	dBm
		3400 MHz ≤ f ≤ 3800 MHz	16	19	-	dBm

- [1] Supply voltage on pins RF_OUT, V_{CC2}, V_{DDA}, V_{CC1} and V_{DDD}.
[2] See [Section 9.2](#).
[3] P_i = −23 dBm per tone; Δf = 10 MHz.
[4] See [Section 11](#).

2. Pinning information

2.1 Pinning



2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 13, 14, 18, 25, 26, 27, 28, 31, 32	Ground
n.c.	11, 30	not connected
RF_OUT	12	RF output and supply to amplifier 2
V _{CC2}	15	Supply voltage to amplifier 2
V _{DDA}	16	Analog supply voltage to DSA

Table 2. Pin description ...continued

Symbol	Pin	Description
V _{CC1}	17	Supply voltage to amplifier 1
V _{DD}	19	Digital supply voltage to digital controller
SER_OUT	20	SPI data output
SS	21	SPI slave select (0 = select; 1 = deselect)
SER_IN	22	SPI data input
CLK	23	SPI clock input
PUPMXG/PWRDN	24	Power-up gain attenuation / power down
RF_IN	29	RF input

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BGA7210	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-3

4. Marking

Table 4. Marking

Type number	Marking code
BGA7210	7210

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{SUP}	supply voltage		[1] -0.6	+8	V
V _I	input voltage		[2] -0.6	+8	V
V _O	output voltage		[3] -0.6	+8	V
I _I	input current		[4] -20	+20	mA
I _O	output current		[5] -20	+20	mA
P _{RFIN}	power on pin RF_IN		-	30	dBm
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		-	150	°C
V _{ESD}	electrostatic discharge voltage	Human Body Model (HBM); According to JEDEC standard 22-A114E	-	4	kV
		Charged Device Model (CDM); According to JEDEC standard 22-C101B	-	2	kV

[1] Absolute maximum DC voltage on pins RF_OUT, V_{CC2}, V_{DDA}, V_{CC1}, V_{DD} and RF_IN.

[2] Absolute maximum DC voltage on pins SS, SER_IN, CLK and PUPMXG/PWRDN.

- [3] Absolute maximum DC voltage on pin SER_OUT.
 [4] Absolute maximum DC current through pins SS, SER_IN, CLK and PUPMXG/PWRDN.
 [5] Absolute maximum DC current through pin SER_OUT.

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	$T_{sp} \leq 85\text{ °C}$	[1] 16	K/W

[1] T_{sp} is the temperature at the solder point.

7. Static characteristics

Table 7. Static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SUP}	supply voltage		[1] 4.75	5.0	5.25	V
$I_{CC(tot)}$	total supply current	maximum	160	195	230	mA
		optimized current	[2] -	185	-	mA
		minimum current	-	120	-	mA
		power-down current	-	15	-	mA
T_{amb}	ambient temperature		-40	+25	+85	°C
I_{CC}	supply current	on pin RF_OUT	-	85	-	mA
	supply current	on pin V_{CC2}	-	45	-	mA
	supply current	on pin V_{DDA}	-	5	-	mA
	supply current	on pin V_{CC1}	-	55	-	mA
	supply current	on pin V_{DDD}	-	5	-	mA
V_{IL}	LOW-level input voltage		[3] -0.1	0	+0.8	V
V_{IH}	HIGH-level input voltage		[3] 2	3.3	$V_{SUP} + 0.1$	V
V_{OL}	LOW-level output voltage		[4] -0.1	0	+0.8	V
V_{OH}	HIGH-level output voltage		[4] 2.5	3.3	3.4	V
I_{OL}	LOW-level output current		[4] -15	-	0	mA
I_{OH}	HIGH-level output current		[4] 0	-	15	mA

[1] Supply voltage on pins RF_OUT, V_{CC2} , V_{DDA} , V_{CC1} and V_{DDD} .

[2] See [Section 9.2](#).

[3] Digital input pins are: SS, SER_IN, CLK and PUPMXG/PWRDN.

[4] Digital output pin is: SER_OUT.

8. Dynamic characteristics

Table 8. Dynamic characteristics

$4.75\text{ V} \leq V_{\text{SUP}} \leq 5.25\text{ V}$; $-40\text{ }^{\circ}\text{C} \leq T_{\text{amb}} \leq +85\text{ }^{\circ}\text{C}$; maximum current; input and output terminated with $50\text{ }\Omega$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	minimum attenuation				
		$700\text{ MHz} \leq f \leq 1400\text{ MHz}$	26	30	33	dB
		$1400\text{ MHz} \leq f \leq 1700\text{ MHz}$	26	29.5	33	dB
		$1700\text{ MHz} \leq f \leq 2200\text{ MHz}$	26	29	33	dB
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	25	28	31	dB
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	22	26	30	dB
$\Delta G/\Delta T$	gain variation with temperature		-0.03	-0.006	0	dB/ $^{\circ}\text{C}$
$\Delta G/\Delta V_{\text{SUP}}$	gain variation with supply voltage		-0.2	-	+0.2	dB/V
α_{range}	attenuation range	$700\text{ MHz} \leq f \leq 2200\text{ MHz}$	28	31.5	35	dB
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	27	30.5	34	dB
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	26	29.5	33	dB
α_{step}	attenuation step	$700\text{ MHz} \leq f \leq 2800\text{ MHz}$	0	0.5	1	dB
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	0	0.5	1.2	dB
ΔG_p	power gain variation	$700\text{ MHz} \leq f \leq 3800\text{ MHz}$	[1] -1.5	-	+1.5	dB
		$700\text{ MHz} \leq f \leq 2200\text{ MHz}$	[2] $-(0.5 + 0.025 \times i_{\alpha})$	-	$+(0.5 + 0.025 \times i_{\alpha})$	dB
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	[2] $-(0.3 + 0.025 \times i_{\alpha})$	-	$+(0.3 + 0.025 \times i_{\alpha})$	dB
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	[2] $-(0.5 + 0.025 \times i_{\alpha})$	-	$+(0.5 + 0.025 \times i_{\alpha})$	dB
$G_{p(\text{flat})}$	power gain flatness	$700\text{ MHz} \leq f \leq 3800\text{ MHz}$; per 200 MHz	-	-	1	dB
RL_{in}	input return loss	$700\text{ MHz} \leq f \leq 3800\text{ MHz}$	10	-	-	dB
RL_{out}	output return loss	$700\text{ MHz} \leq f \leq 3800\text{ MHz}$	7	-	-	dB
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$; $C_{\text{sh}} = 0.68\text{ pF}$	10	-	-	dB
NF	noise figure	minimum attenuation				
		$700\text{ MHz} \leq f \leq 2200\text{ MHz}$	-	6.5	8.5	dB
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	-	7	9	dB
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	-	8	10	dB
		maximum attenuation				
		$700\text{ MHz} \leq f \leq 2200\text{ MHz}$	-	27.5	30.5	dB
		$2200\text{ MHz} \leq f \leq 2800\text{ MHz}$	-	28	31	dB
		$3400\text{ MHz} \leq f \leq 3800\text{ MHz}$	-	28.5	32	dB

Table 8. Dynamic characteristics ...continued

$4.75\text{ V} \leq V_{SUP} \leq 5.25\text{ V}$; $-40\text{ }^{\circ}\text{C} \leq T_{amb} \leq +85\text{ }^{\circ}\text{C}$; maximum current; input and output terminated with $50\text{ }\Omega$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IP _{3O}	output third-order intercept point	minimum attenuation [3]				
		700 MHz $\leq f \leq$ 1400 MHz	34	39	-	dBm
		1400 MHz $\leq f \leq$ 1700 MHz	32	37	-	dBm
		1700 MHz $\leq f \leq$ 2200 MHz	30	35	-	dBm
		2200 MHz $\leq f \leq$ 2800 MHz	28	33	-	dBm
		2200 MHz $\leq f \leq$ 2800 MHz; C _{sh} = 0.68 pF [4]	30	35	-	dBm
		3400 MHz $\leq f \leq$ 3800 MHz	24	27	-	dBm
		maximum attenuation [3]				
		700 MHz $\leq f \leq$ 1400 MHz	-	35	-	dBm
		1400 MHz $\leq f \leq$ 1700 MHz	-	33	-	dBm
		1700 MHz $\leq f \leq$ 2200 MHz	-	31	-	dBm
		2200 MHz $\leq f \leq$ 2800 MHz	-	30	-	dBm
		2200 MHz $\leq f \leq$ 2800 MHz; C _{sh} = 0.68 pF [4]	-	30	-	dBm
		3400 MHz $\leq f \leq$ 3800 MHz	-	25	-	dBm
P _{L(1dB)}	output power at 1 dB gain compression	minimum attenuation				
		700 MHz $\leq f \leq$ 2800 MHz	18	21	-	dBm
		2200 MHz $\leq f \leq$ 2800 MHz; C _{sh} = 0.68 pF [4]	20	23	-	dBm
		3400 MHz $\leq f \leq$ 3800 MHz	16	19	-	dBm
		maximum attenuation				
		700 MHz $\leq f \leq$ 2800 MHz	-	20	-	dBm
		2200 MHz $\leq f \leq$ 2800 MHz; C _{sh} = 0.68 pF [4]	-	20	-	dBm
t _{d(pd)}	power-down delay time	[5]	-	100	-	ns
		[5]	-	5	-	μ s
		[5] [6]	-	100	-	ns

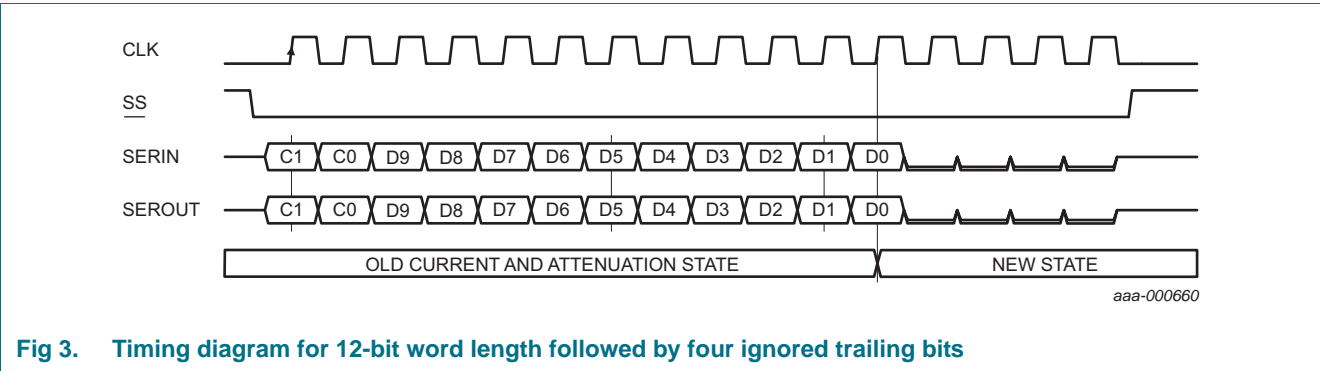
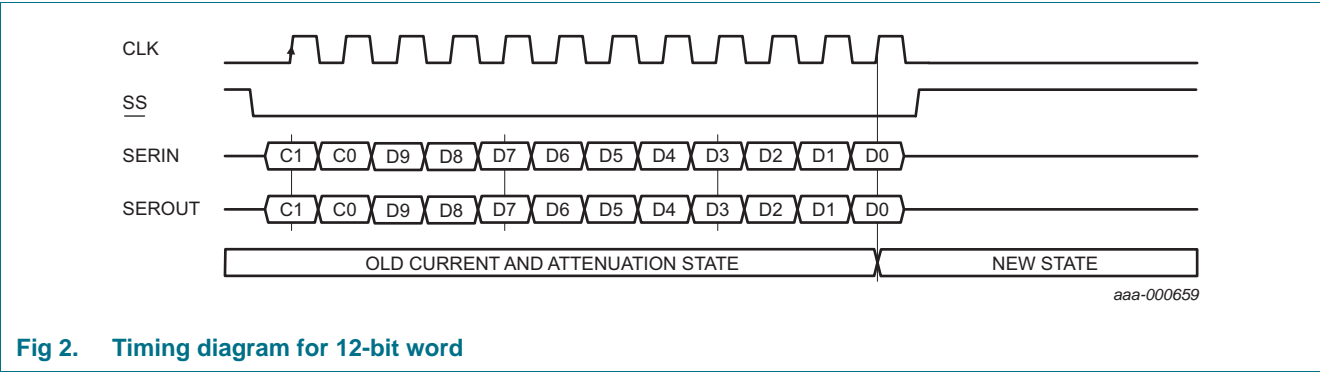
- [1] Normalized to maximum gain and attenuation.
 [2] i_a specifies the decimal attenuation step, ranging from 0 to 63.
 [3] P_i = -23 dBm per tone; Δf = 10 MHz.
 [4] See [Section 11](#).
 [5] To within 0.1 dB of final gain state.
 [6] After last SPI bit is clocked in.

9. Serial Peripheral Interface

9.1 Command word format

The Serial Peripheral Interface (SPI) operates in mode 0. This means that when the SPI is inactive the clock pin is logically LOW. When the SPI interface is active the data is clocked in at the rising edge of the clock pulse; data is clocked out at the negative edge. The

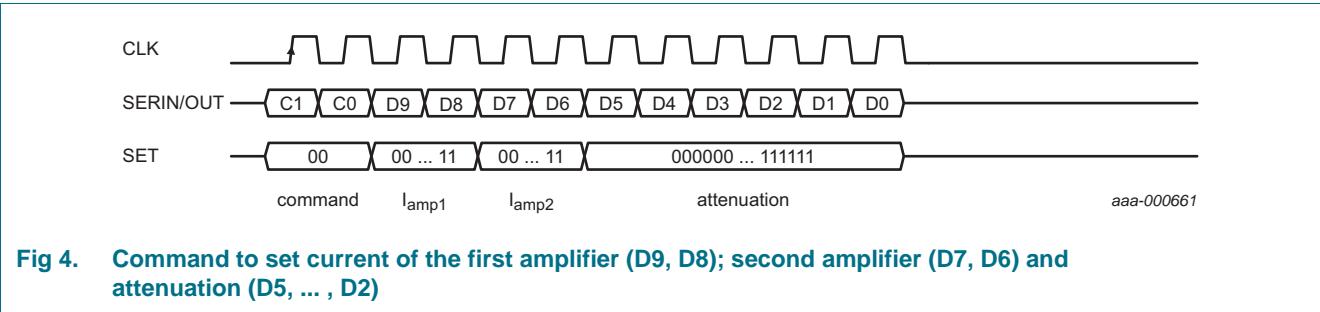
control word length is 12 bits (see [Figure 2](#)), however the word length can be extended appropriately with trailing zeros (see [Figure 3](#)).



The word written on the input (SER_IN) will be replicated on the output (SER_OUT)

9.2 Setting current and attenuation

The current and attenuation are set by bits D9 to D0 and are preceded by the command bits C0 and C1, which are always set to logic LOW, see [Figure 4](#). If all bits are set to logic LOW (0x000) then current is at maximum and attenuation is at minimum; if all bits are set to logic HIGH (0x3FF) then current is at minimum and attenuation is at maximum.



Depending on the attenuation setting the current through the first amplifier and the second amplifier can be optimized, without compromising on linearity. At attenuations less than 9 dB the current in the first amplifier can be reduced with 10 mA; at attenuations equal or larger than 9 dB the current in the second amplifier can be reduced by 15 mA.

Table 9. Current first amplifier truth table

D9, D8	Current reduction (mA)
0x0	0
0x1	-10
0x2	-20
0x3	-30

Table 10. Current second amplifier truth table

D7, D6	Current reduction (mA)
0x0	0
0x1	-15
0x2	-30
0x3	-45

Table 11. Attenuation truth table; major states only

D5, D4, D3, D2, D1, D0	Attenuation (dB)
0x00	0
0x01	0.5
0x02	1
0x04	2
0x08	4
0x10	8
0x20	16
0x3F	31.5

9.3 SPI timing

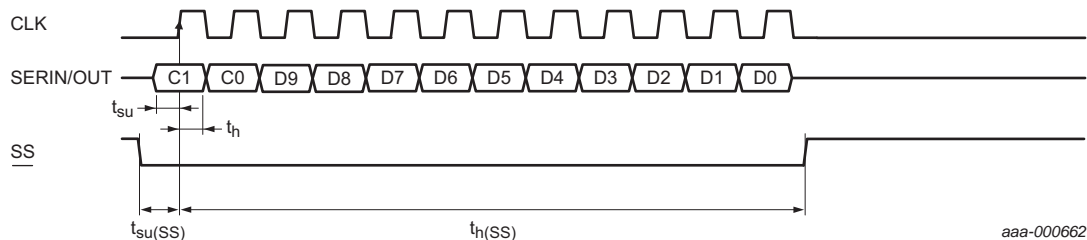


Fig 5. Timing diagram

Table 12. SPI timing

$4.75\text{ V} \leq V_{SUP} \leq 5.25\text{ V}$; $-40\text{ }^{\circ}\text{C} \leq T_{amb} \leq +85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SPI}	SPI frequency		0.1	-	20	MHz
t_{su}	set-up time		10	-	-	ns
t_h	hold time		10	-	-	ns
$t_{su(SS)}$	set-up time on pin SS		10	-	-	ns
$t_{h(SS)}$	hold time on pin SS		$10 + 11 / f_{SPI}$	-	-	ns

10. Power-up and power save

The PUPMXG/PWRDN pin determines the attenuation and currents at start-up of the chip (see [Table 13](#)). After start-up it can be used to power-down the device.

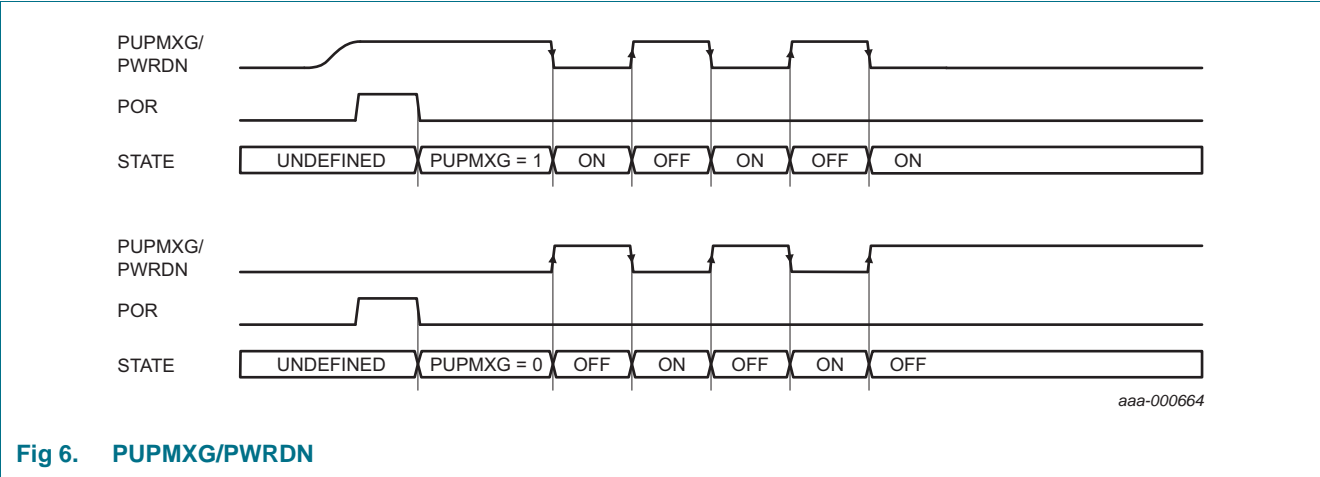


Fig 6. PUPMXG/PWRDN

Table 13. Power-up truth table

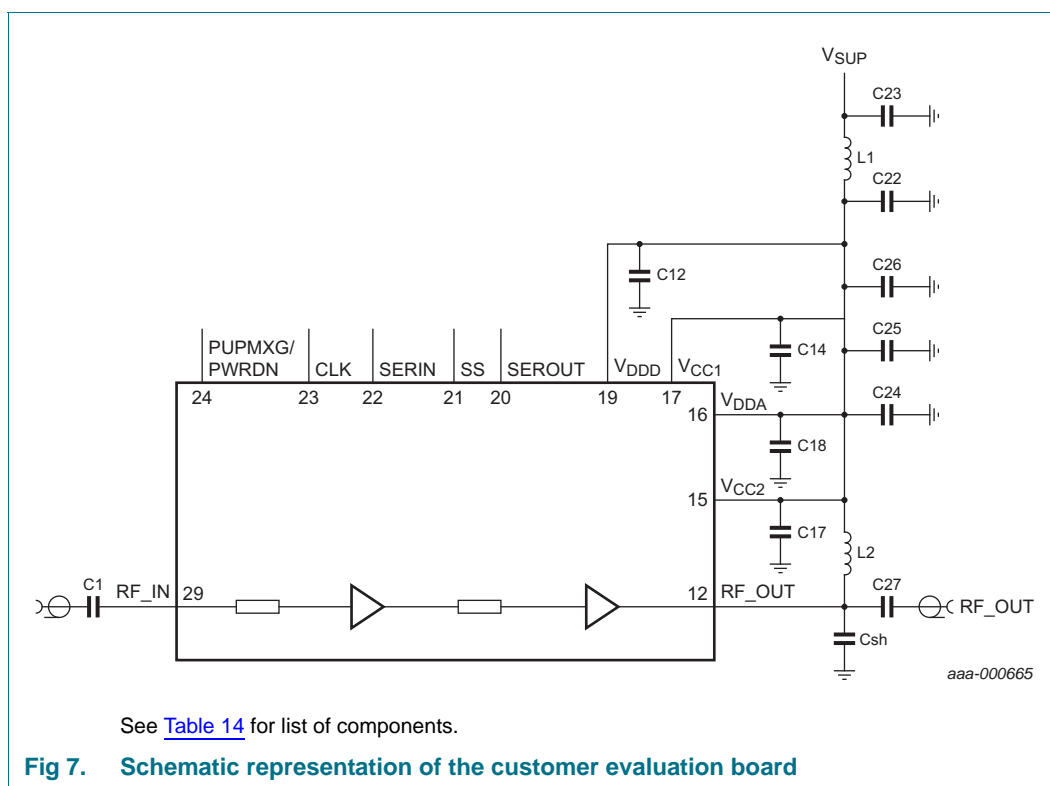
PUPMXG/PWRDN	Current (mA)	Attenuation (dB)
0	120	31.5
1	195	0

11. Application information

11.1 Application board

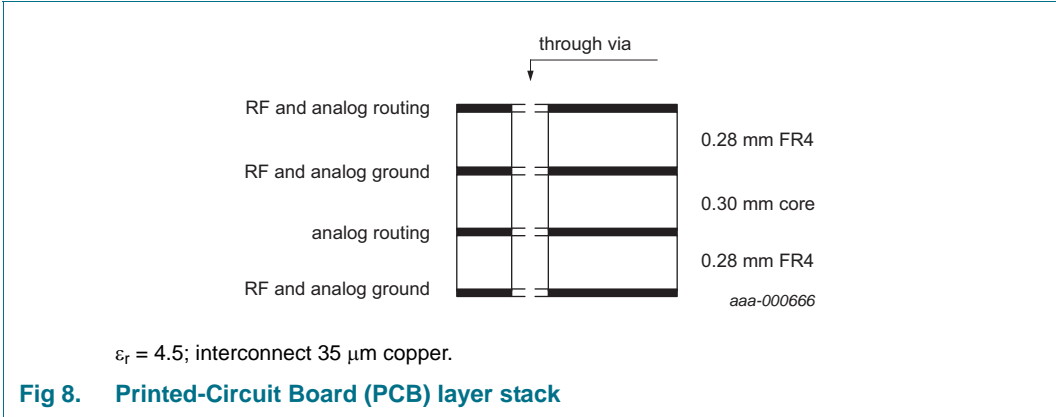
A customer application board is available from NXP upon request. It includes USB interface circuitry and customer software to facilitate evaluation of the BGA7210.

The final application shall be terminated with 50 Ω and decoupled as depicted in [Figure 7](#). The ground leads and exposed paddle should be connected directly to the ground plane. A sufficient number of via holes should be provided to connect the top and bottom ground planes in the final application board. Sufficient cooling should be provided that the temperature of the exposed die pad does not exceed 85 °C.

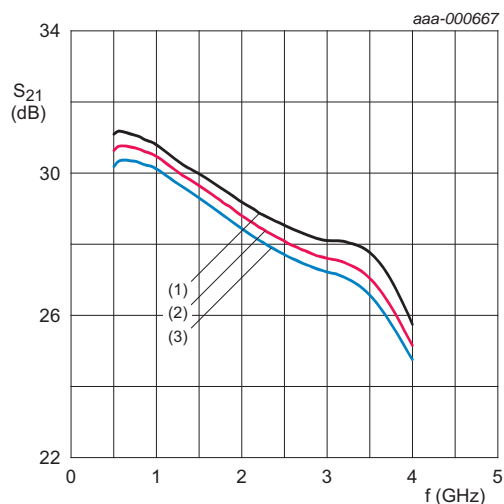
**Table 14. List of components**See [Figure 7](#) for schematics.

Component	Description	Value	Remarks
C1, C27	DC blocking capacitor	100 pF	Murata GRM
C12	decoupling capacitor	100 nF	close to pin 19
C14	decoupling capacitor	100 nF	close to pin 17
C17	decoupling capacitor	100 nF	close to pin 15
C18	decoupling capacitor	100 nF	close to pin 16
C22	optional decoupling capacitor	10 μ F	part of optional ripple filter
C23	optional decoupling capacitor	10 μ F	part of optional ripple filter
C24	decoupling capacitor	100 pF	
C25	decoupling capacitor	100 nF	
C26	decoupling capacitor	4.7 μ F	
C _{sh}	optional matching capacitor to improve linearity at 2.2 GHz to 2.8 GHz	0.68 pF	Murata GRM; shall be located 5.5 mm from pin RF-OUT when using FR4 PCB described below.
L1	optional inductor	820 nH	part of optional ripple filter
L2	inductor	22 nH	Murata LQW 18

The recommended FR4 PCB layer stack is described in [Figure 8](#). A 50 Ω coplanar grounded wave guide can be implemented by a 0.48 mm RF track and a clearance between the track and the ground planes of 1 mm on both sides.



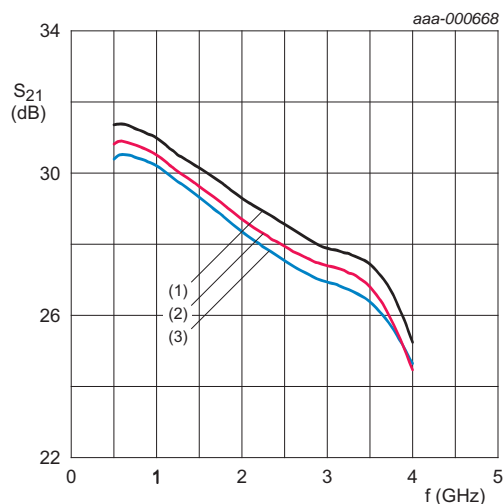
11.2 Characteristics



$V_{SUP} = 5\text{ V}$; maximum current setting.

- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

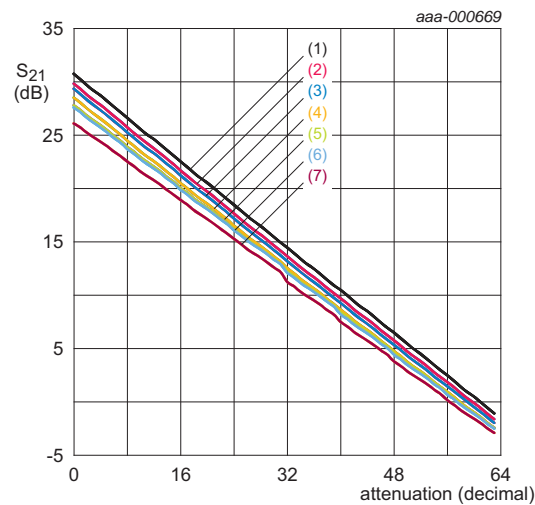
Fig 9. Maximum power gain as a function of frequency; typical values



$V_{SUP} = 5\text{ V}$; maximum current setting and shunt capacitor (C_{sh}).

- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

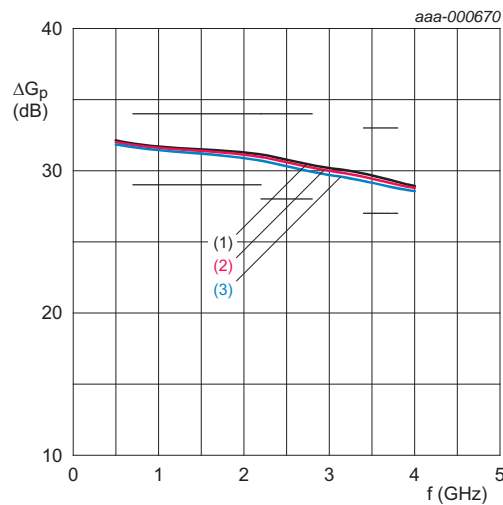
Fig 10. Maximum power gain with shunt capacitor as a function of frequency; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum current setting.

- (1) $f = 0.7\text{ GHz}$
- (2) $f = 1.4\text{ GHz}$
- (3) $f = 1.7\text{ GHz}$
- (4) $f = 2.2\text{ GHz}$
- (5) $f = 2.8\text{ GHz}$
- (6) $f = 2.8\text{ GHz}$ and C_{sh} used
- (7) $f = 3.8\text{ GHz}$

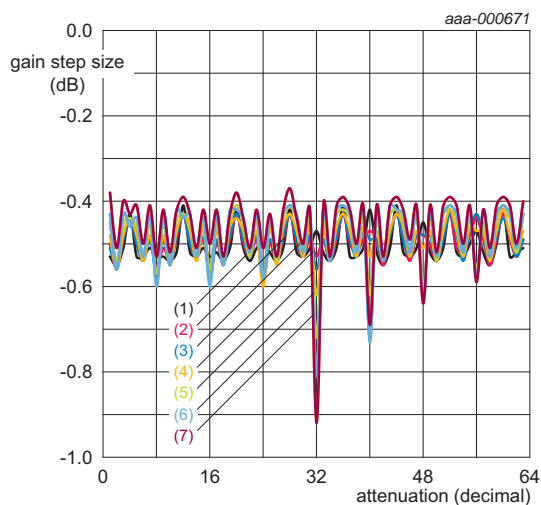
Fig 11. Power gain as a function of attenuation state; typical values



$V_{SUP} = 5\text{ V}$; maximum current setting.

- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

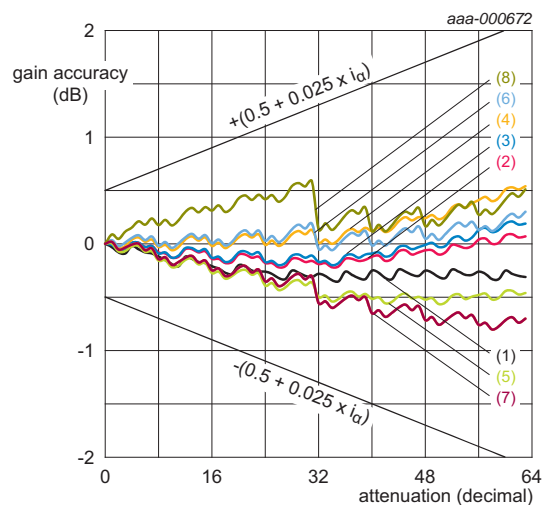
Fig 12. Power gain range as a function of frequency; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; maximum current setting.

- (1) $f = 0.7\text{ GHz}$
- (2) $f = 1.4\text{ GHz}$
- (3) $f = 1.7\text{ GHz}$
- (4) $f = 2.2\text{ GHz}$
- (5) $f = 2.8\text{ GHz}$
- (6) $f = 2.8\text{ GHz}$ and C_{sh} used
- (7) $f = 3.8\text{ GHz}$

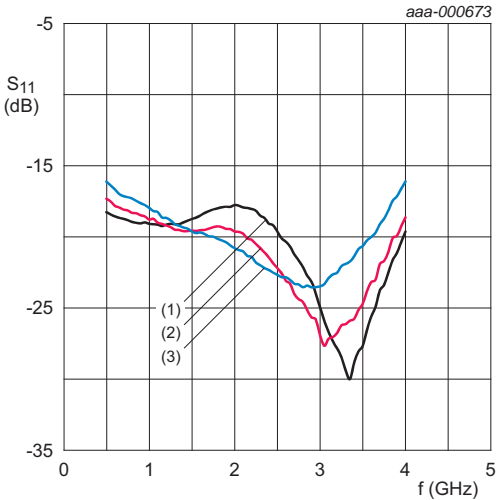
Fig 13. Gain step size as a function of attenuation state; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; maximum current setting.

- (1) $f = 0.7\text{ GHz}$; $\alpha_{range} = 31.5\text{ dB}$
- (2) $f = 1.4\text{ GHz}$; $\alpha_{range} = 31.5\text{ dB}$
- (3) $f = 1.7\text{ GHz}$; $\alpha_{range} = 31.5\text{ dB}$
- (4) $f = 2.2\text{ GHz}$; $\alpha_{range} = 31.5\text{ dB}$
- (5) $f = 2.2\text{ GHz}$; $\alpha_{range} = 30.5\text{ dB}$
- (6) $f = 2.8\text{ GHz}$; $\alpha_{range} = 30.5\text{ dB}$
- (7) $f = 2.8\text{ GHz}$; $\alpha_{range} = 29.5\text{ dB}$
- (8) $f = 3.8\text{ GHz}$; $\alpha_{range} = 29.5\text{ dB}$

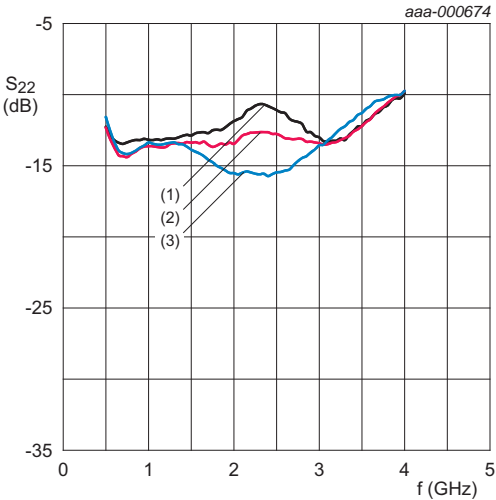
Fig 14. Power gain accuracy as a function of attenuation state; typical values



$V_{SUP} = 5\text{ V}$; maximum current setting;
minimum attenuation.

- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

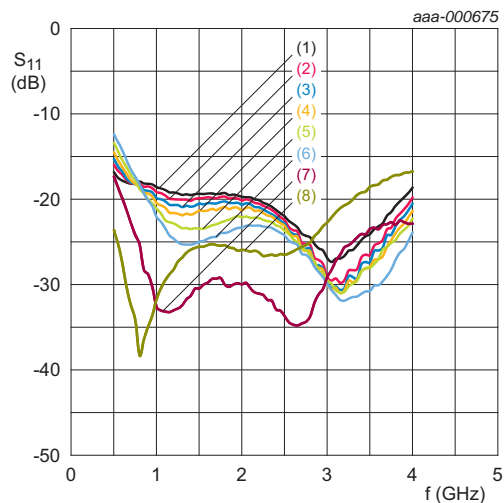
Fig 15. Input return loss as a function of frequency; typical values



$V_{SUP} = 5\text{ V}$; maximum current setting;
minimum attenuation.

- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

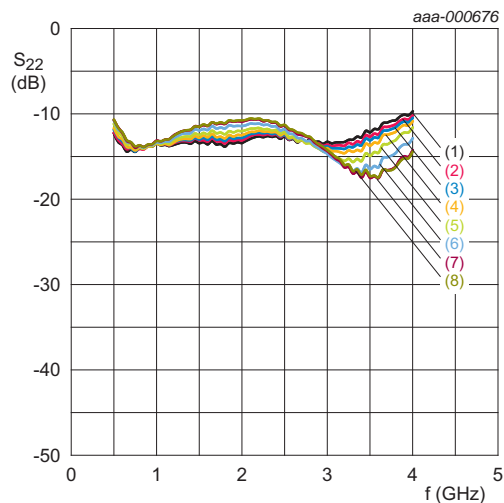
Fig 16. Output return loss as a function of frequency; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum current setting.

- (1) attenuation = 0x00 (minimum)
- (2) attenuation = 0x01
- (3) attenuation = 0x02
- (4) attenuation = 0x04
- (5) attenuation = 0x08
- (6) attenuation = 0x10
- (7) attenuation = 0x20
- (8) attenuation = 0x3F (maximum)

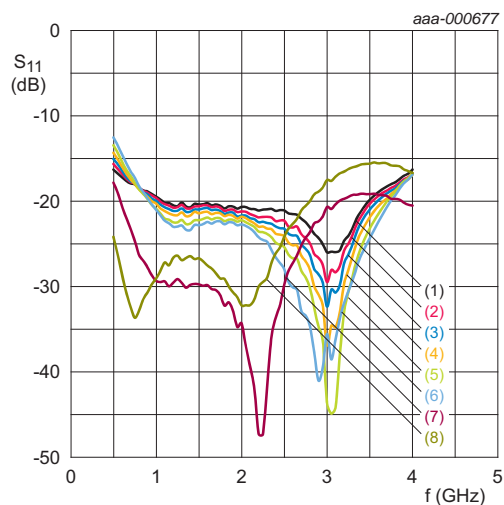
Fig 17. Input return loss as a function of frequency; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum current setting.

- (1) attenuation = 0x00 (minimum)
- (2) attenuation = 0x01
- (3) attenuation = 0x02
- (4) attenuation = 0x04
- (5) attenuation = 0x08
- (6) attenuation = 0x10
- (7) attenuation = 0x20
- (8) attenuation = 0x3F (maximum)

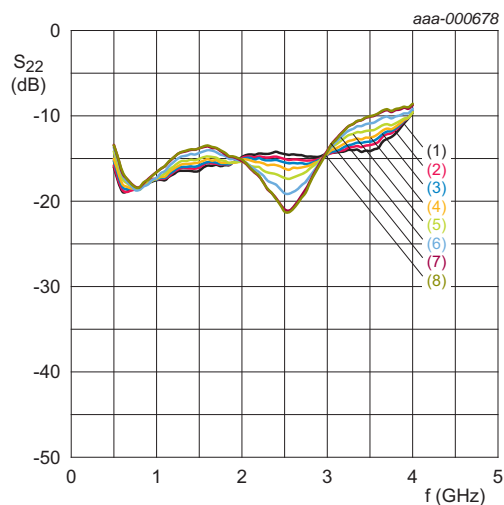
Fig 18. Output return loss as a function of frequency; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum current setting and shunt capacitor (C_{sh}).

- (1) attenuation = 0x00 (minimum)
- (2) attenuation = 0x01
- (3) attenuation = 0x02
- (4) attenuation = 0x04
- (5) attenuation = 0x08
- (6) attenuation = 0x10
- (7) attenuation = 0x20
- (8) attenuation = 0x3F (maximum)

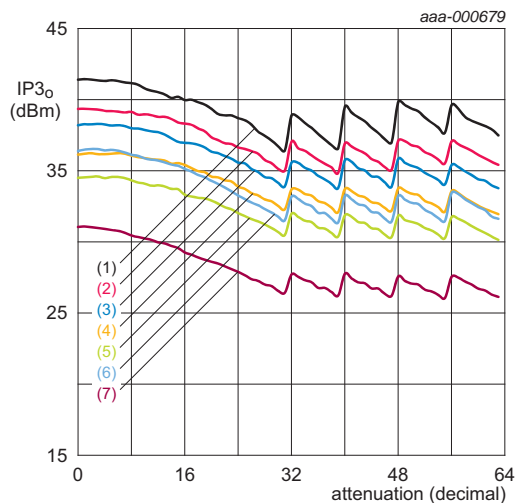
Fig 19. Input return loss with shunt capacitor as a function of frequency; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum current setting and shunt capacitor (C_{sh}).

- (1) attenuation = 0x00 (minimum)
- (2) attenuation = 0x01
- (3) attenuation = 0x02
- (4) attenuation = 0x04
- (5) attenuation = 0x08
- (6) attenuation = 0x10
- (7) attenuation = 0x20
- (8) attenuation = 0x3F (maximum)

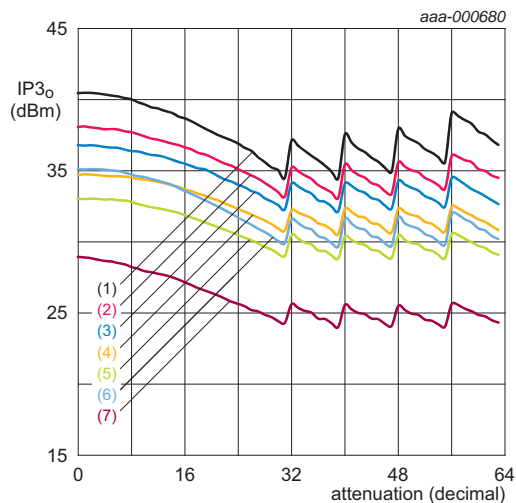
Fig 20. Output return loss with shunt capacitor as a function of frequency; typical values



V_{SUP} = 5 V; T_{amb} = -40 °C; maximum current setting.

- (1) f = 0.7 GHz
- (2) f = 1.4 GHz
- (3) f = 1.7 GHz
- (4) f = 2.2 GHz
- (5) f = 2.8 GHz
- (6) f = 2.8 GHz and C_{sh} used
- (7) f = 3.8 GHz

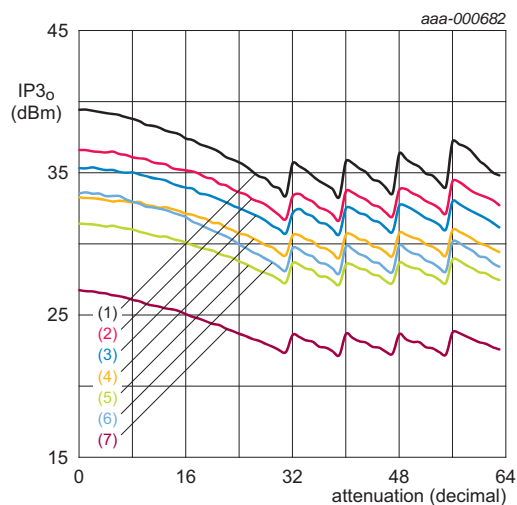
Fig 21. Output third-order intercept point as a function of attenuation state; typical values



V_{SUP} = 5 V; T_{amb} = 25 °C; maximum current setting.

- (1) f = 0.7 GHz
- (2) f = 1.4 GHz
- (3) f = 1.7 GHz
- (4) f = 2.2 GHz
- (5) f = 2.8 GHz
- (6) f = 2.8 GHz and C_{sh} used
- (7) f = 3.8 GHz

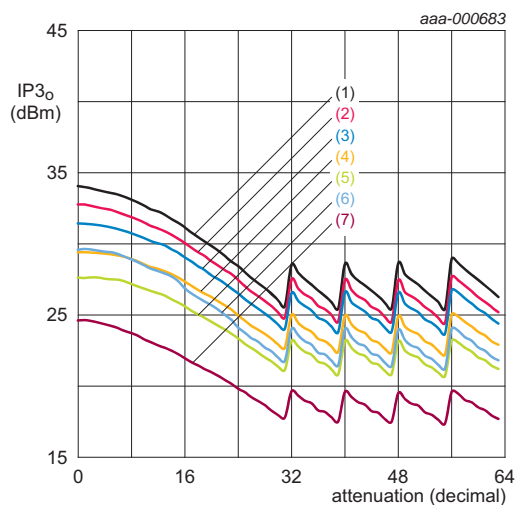
Fig 22. Output third-order intercept point as a function of attenuation state; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 85\text{ °C}$; maximum current setting.

- (1) $f = 0.7\text{ GHz}$
- (2) $f = 1.4\text{ GHz}$
- (3) $f = 1.7\text{ GHz}$
- (4) $f = 2.2\text{ GHz}$
- (5) $f = 2.8\text{ GHz}$
- (6) $f = 2.8\text{ GHz}$ and C_{sh} used
- (7) $f = 3.8\text{ GHz}$

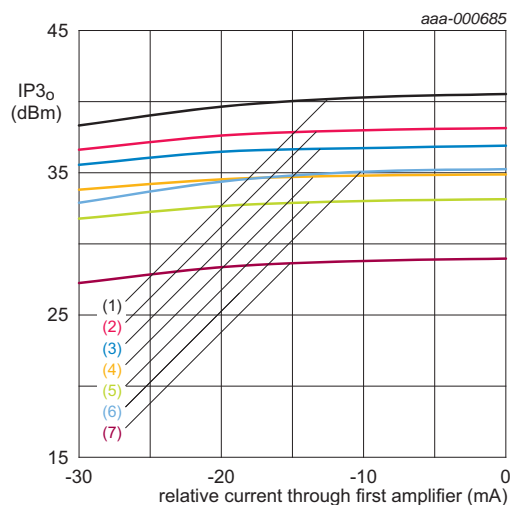
Fig 23. Output third-order intercept point as a function of attenuation state; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; minimal current setting.

- (1) $f = 0.7\text{ GHz}$
- (2) $f = 1.4\text{ GHz}$
- (3) $f = 1.7\text{ GHz}$
- (4) $f = 2.2\text{ GHz}$
- (5) $f = 2.8\text{ GHz}$
- (6) $f = 2.8\text{ GHz}$ and C_{sh} used
- (7) $f = 3.8\text{ GHz}$

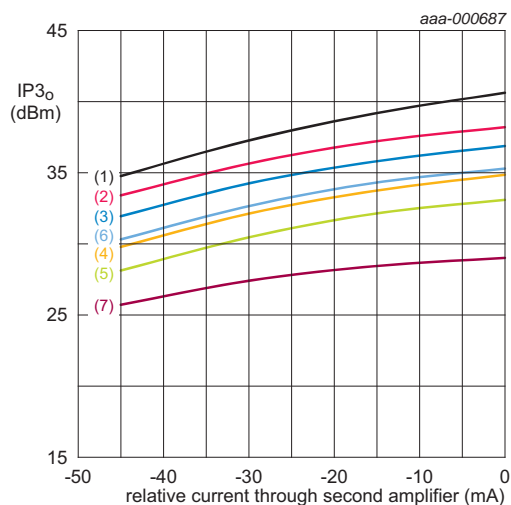
Fig 24. Output third-order intercept point as a function of attenuation state; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; maximum gain;
maximum current through second amplifier.

- (1) $f = 0.7\text{ GHz}$
- (2) $f = 1.4\text{ GHz}$
- (3) $f = 1.7\text{ GHz}$
- (4) $f = 2.2\text{ GHz}$
- (5) $f = 2.8\text{ GHz}$
- (6) $f = 2.8\text{ GHz}$ and C_{sh} used
- (7) $f = 3.8\text{ GHz}$

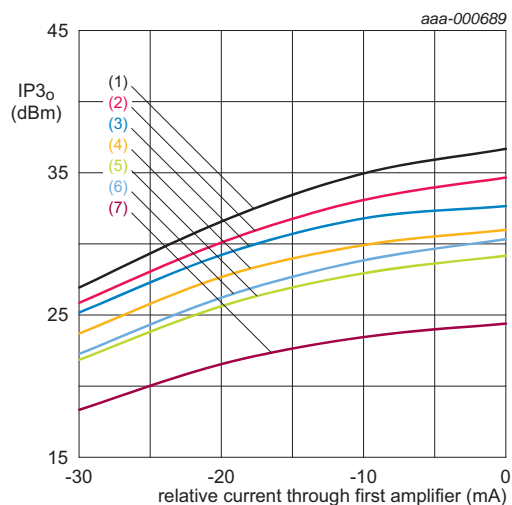
Fig 25. Output third-order intercept point as a function of relative current through first amplifier; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; maximum gain;
maximum current through first amplifier.

- (1) $f = 0.7\text{ GHz}$
- (2) $f = 1.4\text{ GHz}$
- (3) $f = 1.7\text{ GHz}$
- (4) $f = 2.2\text{ GHz}$
- (5) $f = 2.8\text{ GHz}$
- (6) $f = 2.8\text{ GHz}$ and C_{sh} used
- (7) $f = 3.8\text{ GHz}$

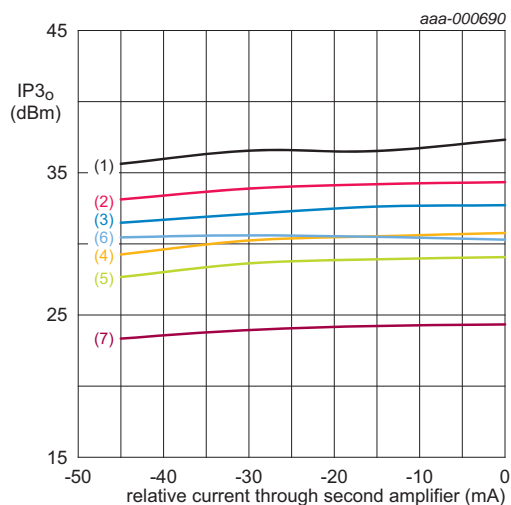
Fig 26. Output third-order intercept point as a function of relative current through second amplifier; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; minimum gain;
maximum current through second amplifier.

- (1) $f = 0.7\text{ GHz}$
- (2) $f = 1.4\text{ GHz}$
- (3) $f = 1.7\text{ GHz}$
- (4) $f = 2.2\text{ GHz}$
- (5) $f = 2.8\text{ GHz}$
- (6) $f = 2.8\text{ GHz}$ and C_{sh} used
- (7) $f = 3.8\text{ GHz}$

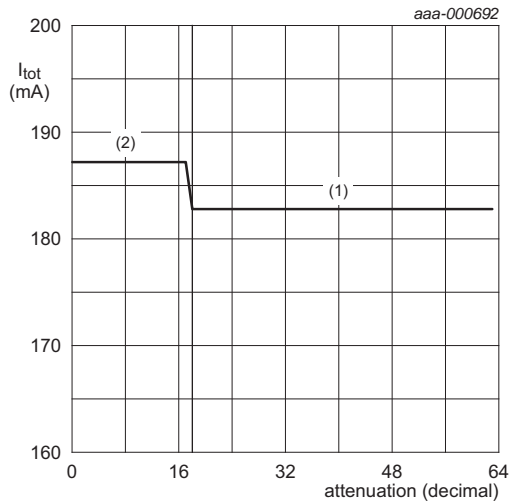
Fig 27. Output third-order intercept point as a function of relative current through first amplifier; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; minimum gain;
maximum current through first amplifier.

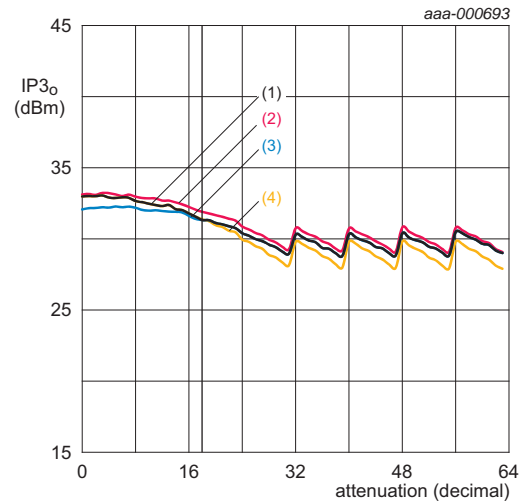
- (1) $f = 0.7\text{ GHz}$
- (2) $f = 1.4\text{ GHz}$
- (3) $f = 1.7\text{ GHz}$
- (4) $f = 2.2\text{ GHz}$
- (5) $f = 2.8\text{ GHz}$
- (6) $f = 2.8\text{ GHz}$ and C_{sh} used
- (7) $f = 3.8\text{ GHz}$

Fig 28. Output third-order intercept point as a function of relative current through second amplifier; typical values



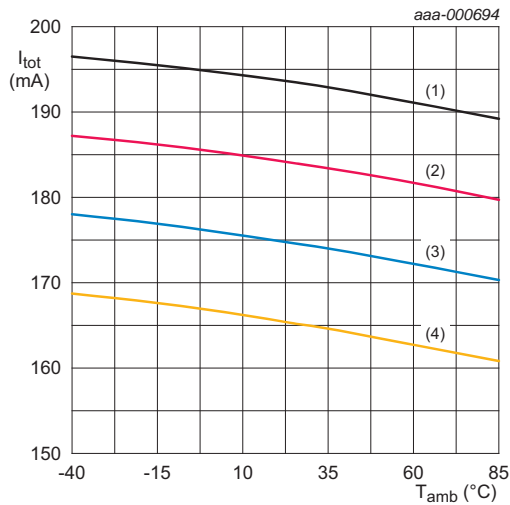
- $V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- (1) $\Delta I_{AMP1} / \Delta I_{AMP2} = 0\text{ mA} / -15\text{ mA}$
 - (2) $\Delta I_{AMP1} / \Delta I_{AMP2} = -10\text{ mA} / 0\text{ mA}$

Fig 29. Total current as a function of attenuation state optimized for IP_{3O} ; typical values



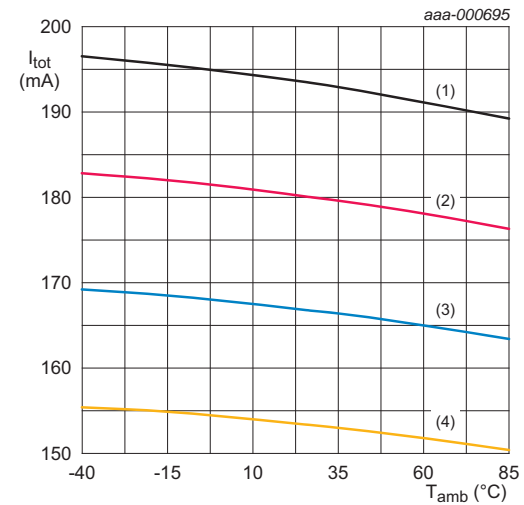
- $V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $f = 2.8\text{ GHz}$.
- (1) $\Delta I_{AMP1} / \Delta I_{AMP2} = I_{opt}$
 - (2) $\Delta I_{AMP1} / \Delta I_{AMP2} = 0\text{ mA} / 0\text{ mA}$
 - (3) $\Delta I_{AMP1} / \Delta I_{AMP2} = 0\text{ mA} / -15\text{ mA}$
 - (4) $\Delta I_{AMP1} / \Delta I_{AMP2} = -10\text{ mA} / 0\text{ mA}$

Fig 30. Output third-order intercept point as a function of attenuation state; typical values



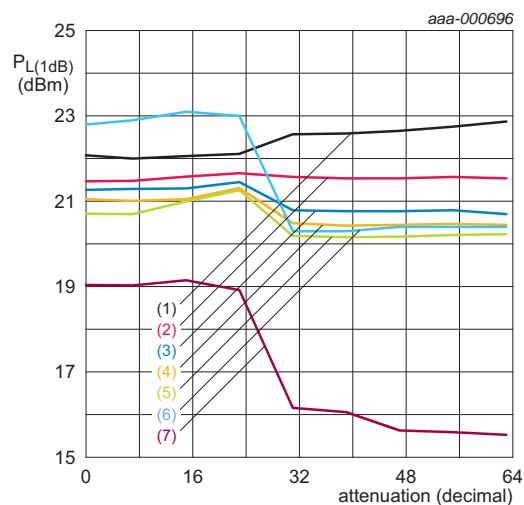
- $V_{SUP} = 5\text{ V}$; maximum current through second amplifier.
- (1) $I_{AMP1} = 0\text{ mA}$
 - (2) $I_{AMP1} = -10\text{ mA}$
 - (3) $I_{AMP1} = -20\text{ mA}$
 - (4) $I_{AMP1} = -30\text{ mA}$

Fig 31. Total current as a function of ambient temperature; typical values



- $V_{SUP} = 5\text{ V}$; maximum current through first amplifier.
- (1) $I_{AMP2} = 0\text{ mA}$
 - (2) $I_{AMP2} = -10\text{ mA}$
 - (3) $I_{AMP2} = -20\text{ mA}$
 - (4) $I_{AMP2} = -30\text{ mA}$

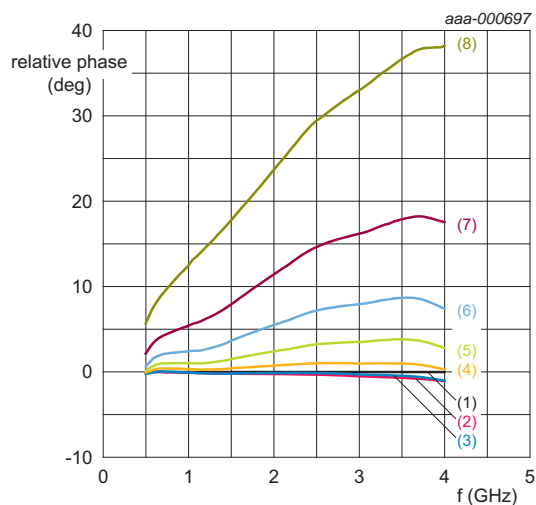
Fig 32. Total current as a function of ambient temperature; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 85\text{ }^{\circ}\text{C}$; maximum current setting; attenuation states 0, 7, 15, 23, 31, 39, 47, 55 and 63 are depicted.

- (1) $f = 0.7\text{ GHz}$
- (2) $f = 1.4\text{ GHz}$
- (3) $f = 1.7\text{ GHz}$
- (4) $f = 2.2\text{ GHz}$
- (5) $f = 2.8\text{ GHz}$
- (6) $f = 2.8\text{ GHz}$ and C_{sh} used
- (7) $f = 3.8\text{ GHz}$

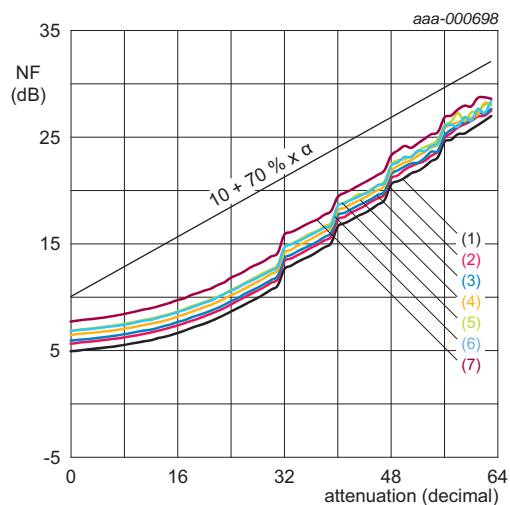
Fig 33. Output power at 1 dB gain compression as a function of attenuation state; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum current setting.

- (1) attenuation = 0x00 (minimum)
- (2) attenuation = 0x01
- (3) attenuation = 0x02
- (4) attenuation = 0x04
- (5) attenuation = 0x08
- (6) attenuation = 0x10
- (7) attenuation = 0x20
- (8) attenuation = 0x3F (maximum)

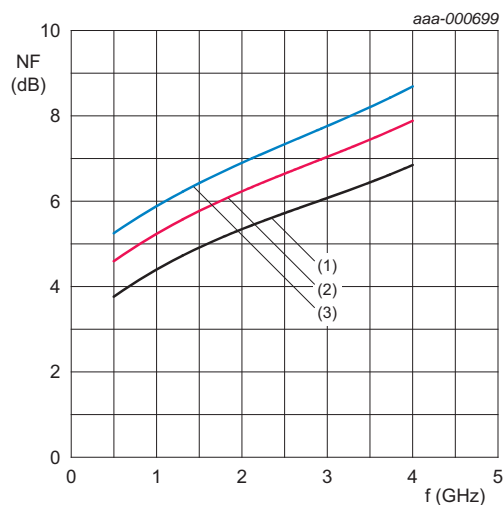
Fig 34. Relative phase as a function of frequency; typical values



$V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum current setting.

- (1) $f = 0.7\text{ GHz}$
- (2) $f = 1.4\text{ GHz}$
- (3) $f = 1.7\text{ GHz}$
- (4) $f = 2.2\text{ GHz}$
- (5) $f = 2.8\text{ GHz}$
- (6) $f = 2.8\text{ GHz}$ and C_{sh} used
- (7) $f = 3.8\text{ GHz}$

Fig 35. Noise figure as a function of attenuation state; typical values



$V_{SUP} = 5\text{ V}$; maximum gain and maximum current setting.

- (1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
- (2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
- (3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

Fig 36. Noise figure as a function of frequency; typical values

12. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads;
32 terminals; body 5 x 5 x 0.85 mm

SOT617-3

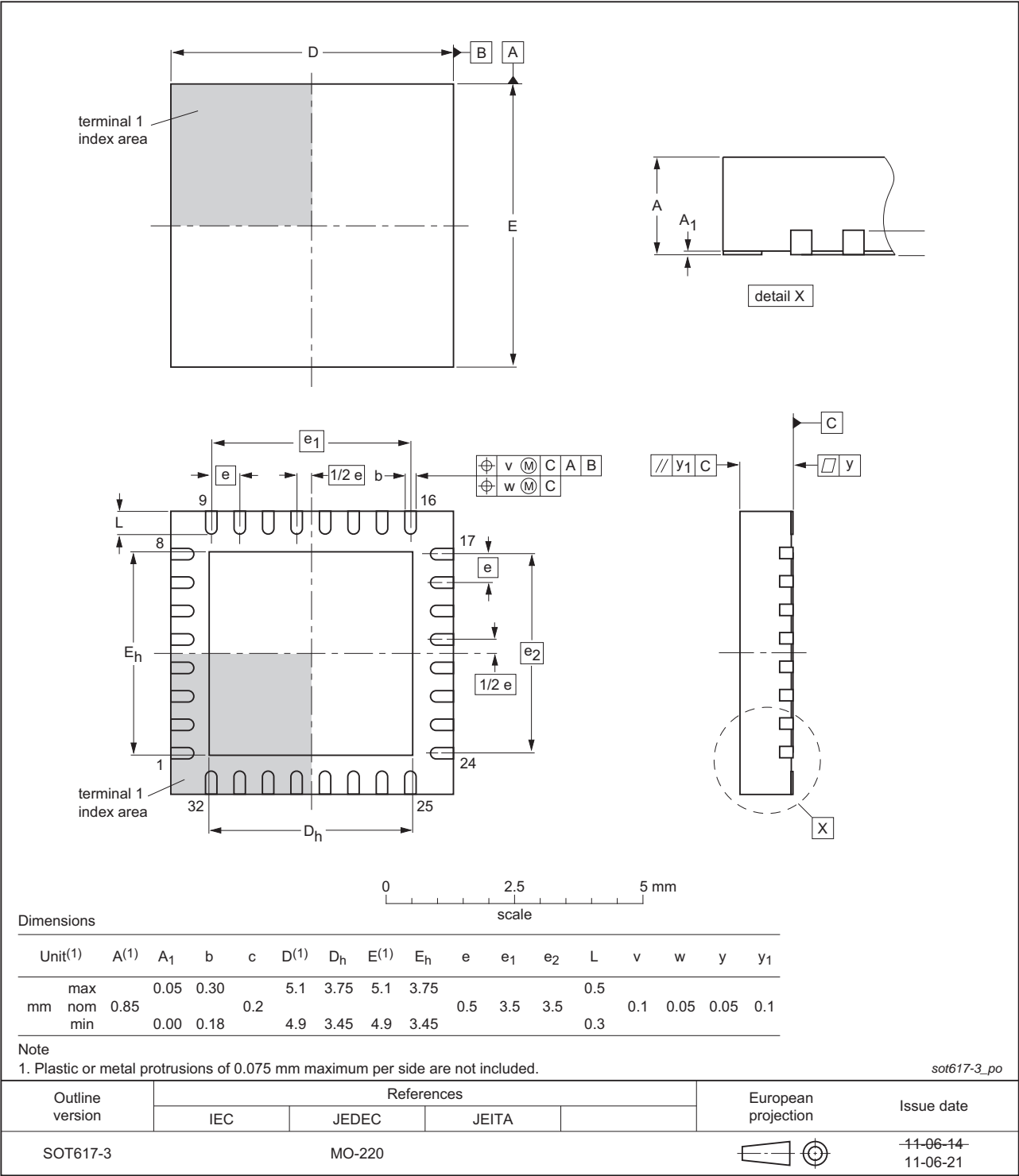


Fig 37. Package outline SOT617-3 (HVQFN32)

13. Packing information

The BGA7210 will be delivered in reel pack SMD 7", 1500 pieces per reel.

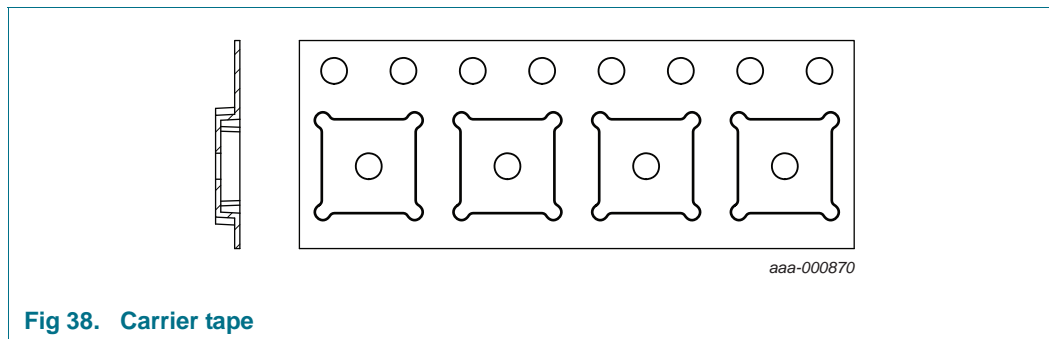


Fig 38. Carrier tape

14. Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
DSA	Digital Step Attenuator
HBM	Human Body Model
IF	Intermediate Frequency
MMIC	Monolithic Microwave Integrated Circuit
POR	Power-On Reset
RF	Radio Frequency
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
WiMAX	Worldwide Interoperability for Microwave Access

15. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGA7210 v.5	20170120	Product data sheet	-	BGA7210 v.4
Modifications:	<ul style="list-style-type: none"> • Section 1: added BTS6001A according to our new naming convention 			
BGA7210 v.4	20130128	Product data sheet	-	BGA7210 v.3
Modifications:	<ul style="list-style-type: none"> • Table 4: updated. 			
BGA7210 v.3	20121224	Product data sheet	-	BGA7210 v.2
BGA7210 v.2	20120104	Product data sheet	-	BGA7210 v.1
BGA7210 v.1	20111213	Preliminary data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	2
2	Pinning information	3
2.1	Pinning	3
2.2	Pin description	3
3	Ordering information	4
4	Marking	4
5	Limiting values	4
6	Thermal characteristics	5
7	Static characteristics	5
8	Dynamic characteristics	6
9	Serial Peripheral Interface	8
9.1	Command word format	8
9.2	Setting current and attenuation	8
9.3	SPI timing	10
10	Power-up and power save	10
11	Application information	11
11.1	Application board	11
11.2	Characteristics	13
12	Package outline	26
13	Packing information	27
14	Abbreviations	27
15	Revision history	27
16	Legal information	28
16.1	Data sheet status	28
16.2	Definitions	28
16.3	Disclaimers	28
16.4	Trademarks	29
17	Contact information	29
18	Contents	30

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2017.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 20 January 2017

Document identifier: BGA7210